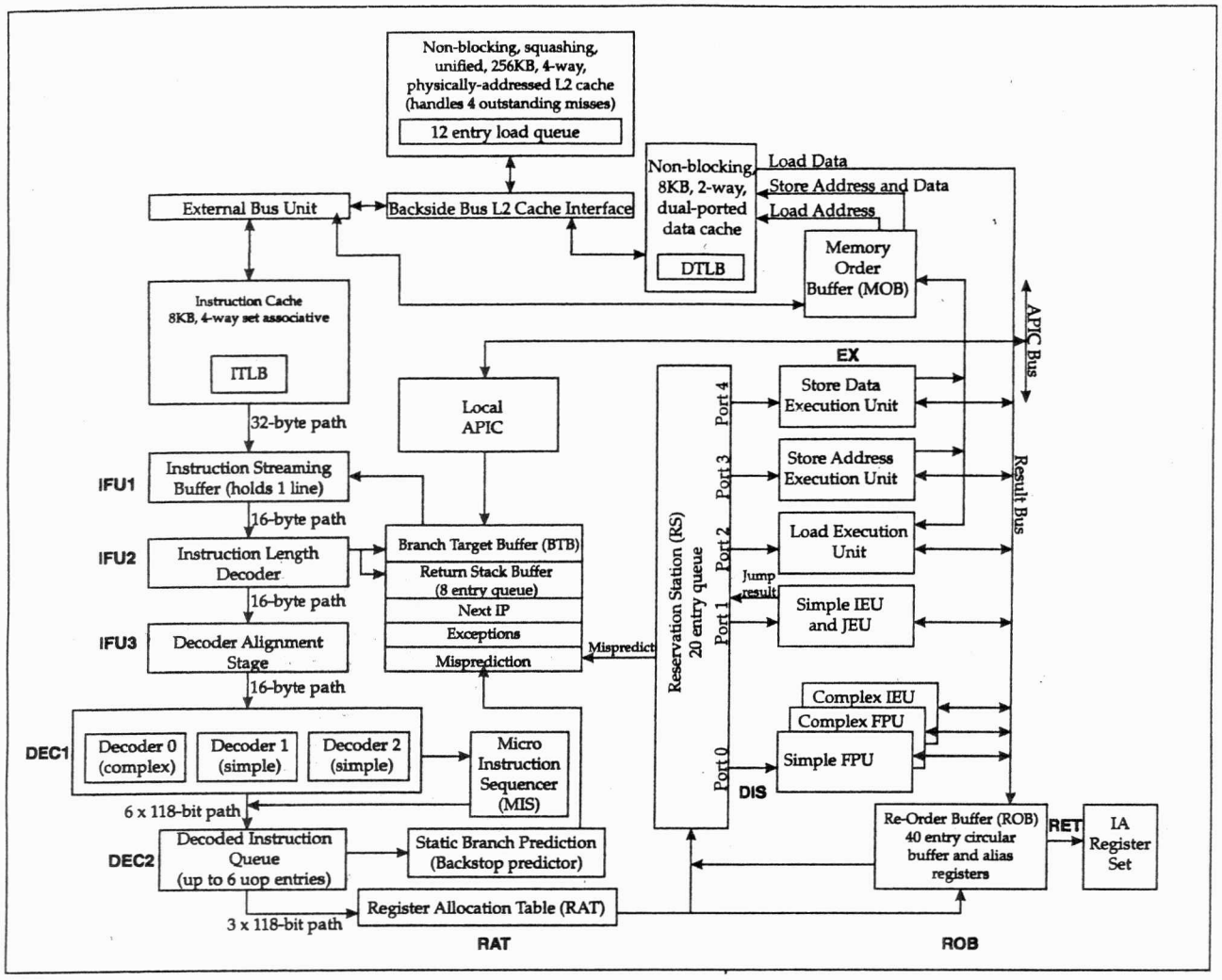


Figure 5-18: Fetch/Decode/Execute Engine

Pentium Pro and Pentium II System Architecture

Figure 5-2: Example Instructions in Memory

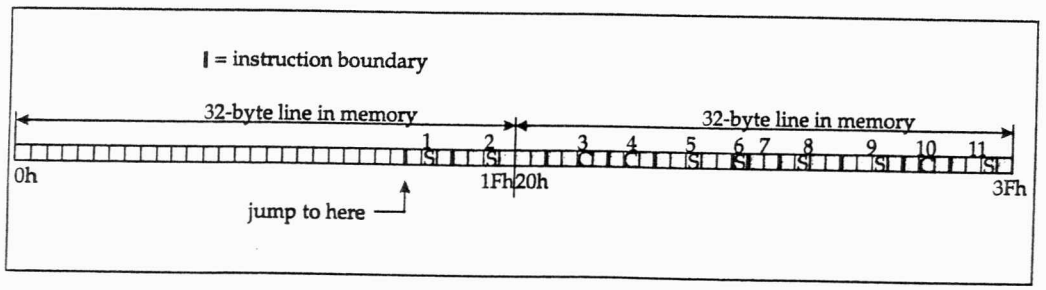
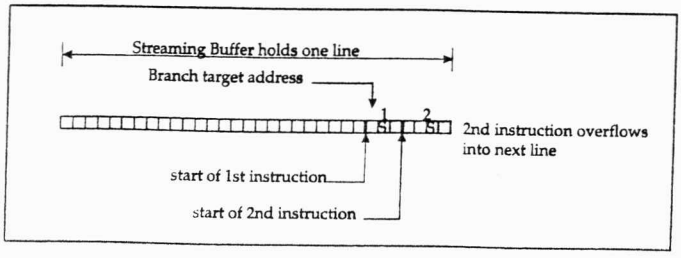
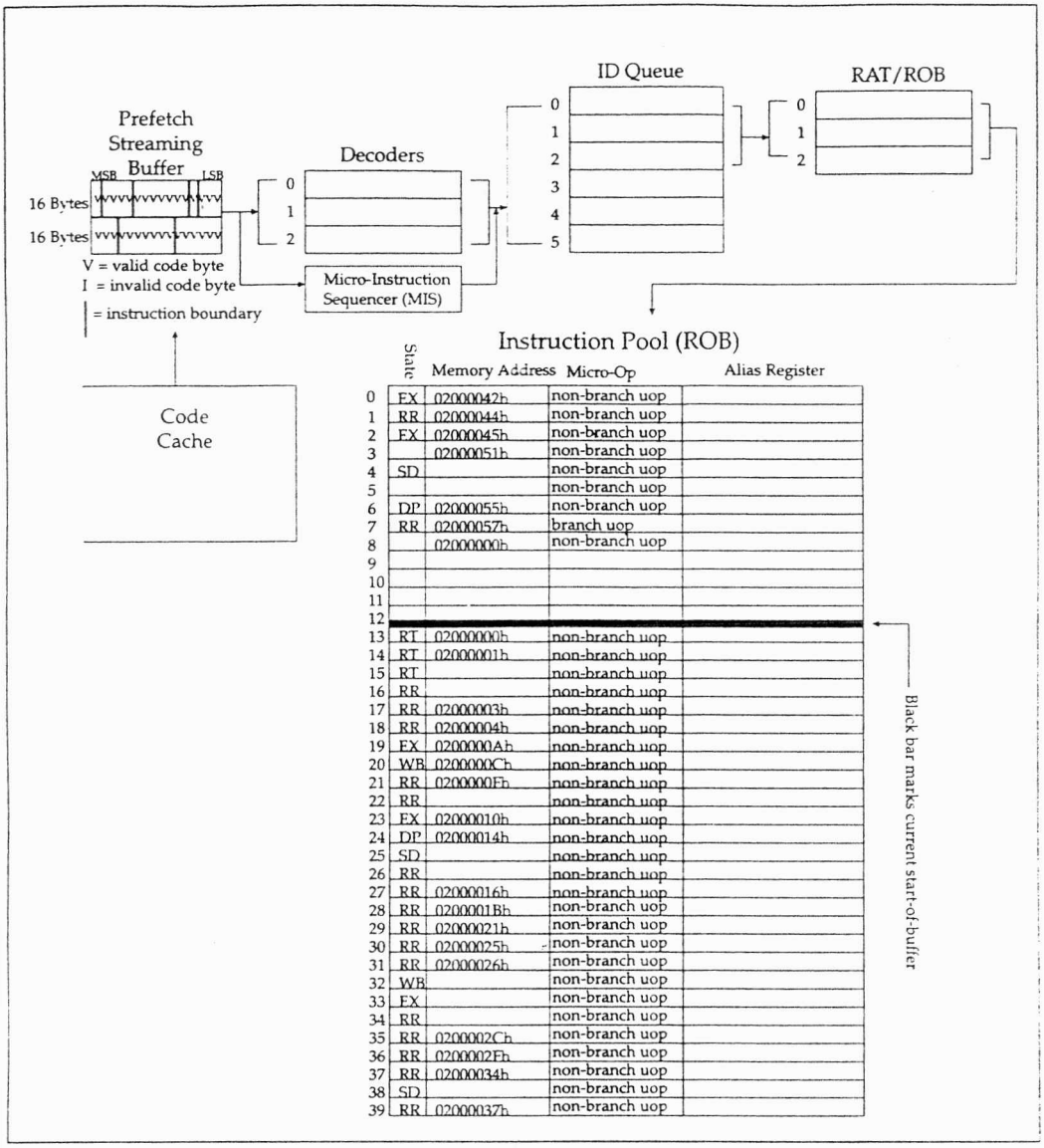


Figure 5-3: Contents of Prefetch Streaming Buffer Immediately after Line Fetched





SD scheduled for execution
DP to be Dispatched to its port
EX
WB
RR ready for retirement
RT being retired