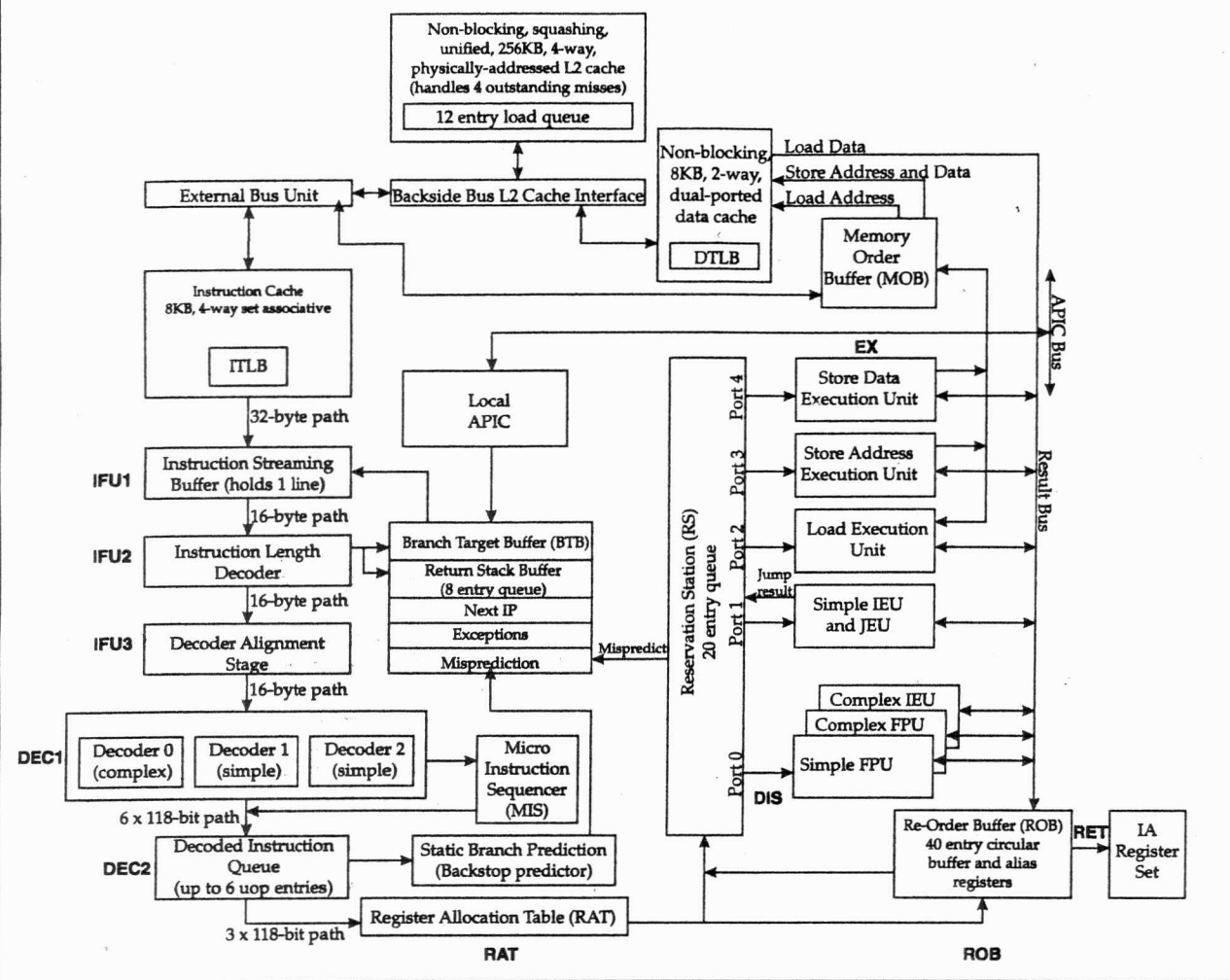


Figure 5-18: Fetch/Decode/Execute Engine



Pentium Pro and Pentium II System Architecture

Figure 5-2: Example Instructions in Memory

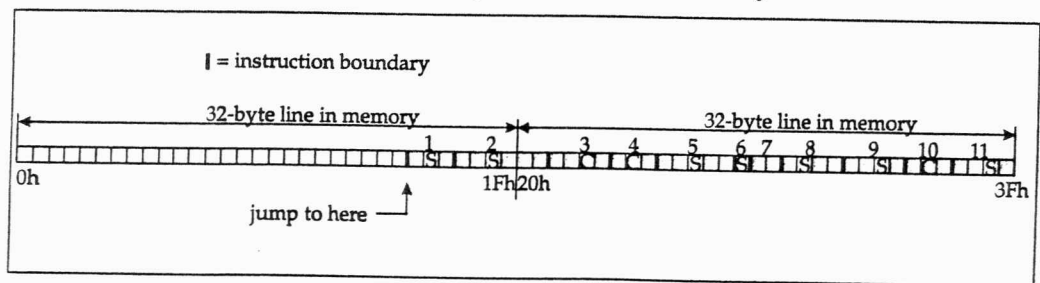
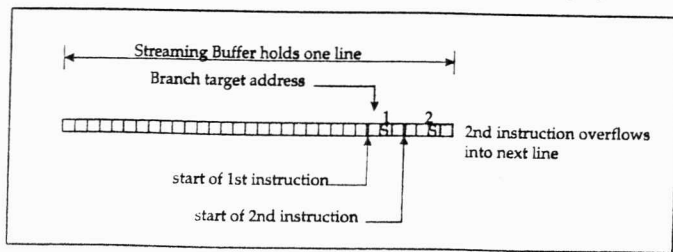
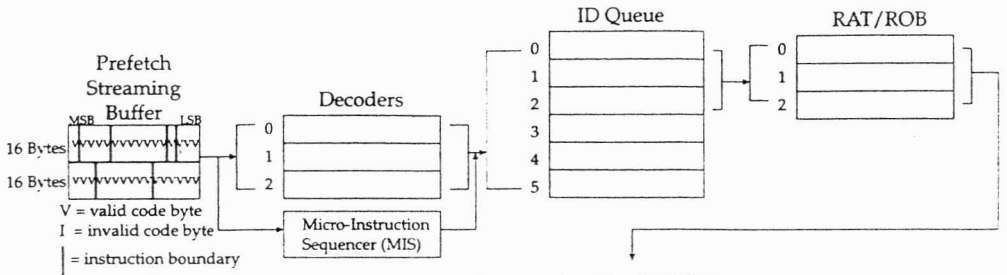


Figure 5-3: Contents of Prefetch Streaming Buffer Immediately after Line Fetched





Instruction Pool (ROB)

Slot	Memory Address	Micro-Op	Alias Register
0	EX 02000042h	non-branch uop	
1	RR 02000044h	non-branch uop	
2	EX 02000045h	non-branch uop	
3	02000051h	non-branch uop	
4	SD	non-branch uop	
5		non-branch uop	
6	DP 02000055h	non-branch uop	
7	RR 02000057h	branch uop	
8	02000000h	non-branch uop	
9			
10			
11			
12			
13	RT 02000000h	non-branch uop	
14	RT 02000001h	non-branch uop	
15	RT	non-branch uop	
16	RR	non-branch uop	
17	RR 02000003h	non-branch uop	
18	RR 02000004h	non-branch uop	
19	EX 0200000Ah	non-branch uop	
20	WB 0200000Ch	non-branch uop	
21	RR 0200000Fh	non-branch uop	
22	RR	non-branch uop	
23	EX 02000010h	non-branch uop	
24	DP 02000014h	non-branch uop	
25	SD	non-branch uop	
26	RR	non-branch uop	
27	RR 02000016h	non-branch uop	
28	RR 0200001Bh	non-branch uop	
29	RR 02000021h	non-branch uop	
30	RR 02000025h	non-branch uop	
31	RR 02000026h	non-branch uop	
32	WB	non-branch uop	
33	EX	non-branch uop	
34	RR	non-branch uop	
35	RR 0200002Ch	non-branch uop	
36	RR 0200002Fh	non-branch uop	
37	RR 02000034h	non-branch uop	
38	SD	non-branch uop	
39	RR 02000037h	non-branch uop	

Black bar marks current start-of-buffer

SD scheduled for execution
 DP to be dispatched to its port
 EX
 WB
 RR ready for which must
 RT begin which