# Syllabus Attività Formativa

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| **Anno Offerta** | 2022 |
| **Corso di Studio** | 06415 - COMPUTER ENGINEERING |
| **Regolamento Didattico** | 06415-1222 |
| **Percorso di Studio** | 00 - PERCORSO COMUNE |
| **Insegnamento/Modulo** | 504712 - ADVANCED COMPUTER ARCHITECTURE - ADVANCED COMPUTER ARCHITECTURE |
| **Attività Formativa Integrata** | - |
| **Partizione Studenti** | - |
| **Periodo Didattico** | S1 - Primo Semestre |
| **Sede** | |
| **Anno Corso** | 1 |
| **Settore** | ING-INF/05 - SISTEMI DI ELABORAZIONE DELLE INFORMAZIONI |
| **Tipo attività Formativa** | B - Caratterizzante |
| **Ambito** | 50369 - Ingegneria informatica |
| **CFU** | 6.0 |
| **Ore Attività Frontali** | 62.0 |
| **AF_ID** | 412543 |

| Tipo Testo | Codice Tipo Testo | Num. Max. Caratteri | Obbl. | Testo in Italiano | Testo in Inglese |
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| **Lingua insegnamento** | LINGUA_INS | 8000 | Sì | INGLESE | English |
| **Prerequisiti** | PREREQ | 8000 | No | | Basic understanding of computer architecture: Von-Neumann machine, CU, busses, memory architecture and addressing modes. Elementary assembly language. Knowledge of the MIPS architecture and instruction set. Basic notions on operating systems: process, thread, mutual exclusion. The C-language is required for the programming lab and associated project. |
| **Obiettivi formativi e risultati di apprendimento** | OBIETT_FORM | 8000 | Sì | | The course describes the architecture of modern processors and multi-processors and introduces the principles of parallel programming. The student will understand the principle of operation of current processors and will be able to assess the distinctive features of general purpose vs embedded microprocessors vs special purpose accelerators (GPUs & tensor flow processors). The emerging multi-core paradigm, the associated shared-memory architecture will be discussed, as well as distributed memory one. The latter will be the basis for a parallel programming project to be developed in MPI. |

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| | | | | | The Google Cloud platform will be used for instantiating VMs with enough cores to effectively test the parallel project. |
| **Programma e contenuti** | CONTENUTI | 8000 | Sì | | The course is split into two major areas: a description of the architectures and a laboratory on parallel programming. Part I - The processor. This part of the course introduces the basic concepts underlining the design of modern processors. The Instruction Set Architecture (ISA). A Taxonomy for ISAs: CISC, RISC, general purpose, embedded, multimedia, thread & tensors. Basic pipelining: control, hazards, exceptions. Superscalar pipelines: static multiple issue, the VLIW approach. Dynamic scheduling, speculative execution. Compiler support and software optimization. Caches and memory hierarchy: locality. Structure and organization: direct mapping, associativity. Pipelined and multi-level caches. Part II - Multi-processors. A review of multi-processors and parallel architectures, with emphasis on multi-core processors. Parallel processing: SIMD, MIMD, data parallelism, thread parallelism, coarse-grain parallelism. Parallel architectures: shared-memory, distributed memory, clusters. GPU and tensors flow architectures. Part III - Parallel |

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| | | | | | programming. An introduction to parallel processing, with hands-on lab on MPI. The available paradigms: SMP, MPI, graphics and CUDA. The OpenMp standard (hints) |
| **Metodi didattici** | METODI_DID | 8000 | Sì | | Lectures (hours/year in lecture theatre): 32. Practical class (hours/year in lecture theatre): 12. Practicals / Workshops (hours/year in a lab): 18.<br>Lectures are delivered through presentations posted on the course web site. |
| **Testi di riferimento** | TESTI_RIF | 8000 | Sì | | 1) Ferretti, D. Gunetti. Course charts (in pdf). available for download form the course website<br>2) J. L. Hennessy & D. A. Patterson. Computer Architecture: A Quantitative Approach, 3rd - 4rth and 5th editions. Elsevier - Morgan Kaufmann. See detailed instructions on the course website for editions and chapters to be used.<br>3) D. A. Patterson & J. L. Hennessey. Computer Organization and Design: The Hardware/Software Interface, Revised 4th Edition. Morgan Kauffman. See deteiled instruction in the Course website for chapters to be used. |

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| **Modalità di verifica dell'apprendimento** | MOD_VER_APPR | 8000 | Sì | | The final assessment consists of a parallel programming project, of a discussion of the project and of a written test (oral examination is optional). Written test and project each weight 50% in final grade. They can be taken in any order and separately. The project should be prepared by a group of two persons at the most. While the written test can be taken by each individual, project delivery and discussion must be taken by all participant in the group. |
| **Altre informazioni** | ALTRO | 8000 | No | | Free access for a limited amount of computing resources to the Google Cloud Platform will be made available to registered students to develop the final project. Credential will be distributed in due time, must be activated within two months, and expired in 12 months from activation. |
| **Obiettivi Agenda 2030 per lo sviluppo sostenibile** | OB_SVIL_SOS | 4000 | No | | |