Advanced Computer Architecture  
22-01-2019

A) A processor embeds two cores that have private L1 and L2 caches, L3 is shared. The caches obey the MESI protocol and have the following structure: 32KB, 4-way L1 I-cache and D-cache, each 32-byte block; 1024KB, 8-way associative, 64-byte block L2 cache; 4MB, 8-way associative, 64-byte block L3 cache. The latencies (disregarding virtual memory TLB) expressed in clock cycles are: 2 in L1, 6 in L2, 12 in L3. Addresses are 48-bit long. Write operations are managed with a write-back policy. Assuming initially empty and invalidated cache lines throughout the hierarchy, consider the following memory accesses:

core 1) ST F1, 0000FFFFA000hex; (8-byte store)

core 1) LD F2, 0000FFFFA0A0hex; (8-byte load)

core 2) ST F1, 0000FFFFA000hex; (8-byte store)

core 2) ST F3, 0000FFFFA0A0hex; (8-byte store)

a1) show the blocks involved in each cache, and the associated MESI state after each instruction.

B) Let us consider the following code fragment of compiler-unscheduled instructions:

ADDI R1,R0,0000FFFFA000hex -- R1 set to base address 0000FFFFA000hex

loop: LD F1,0(R1)

LD F3,8(R1)

MULTF F2,F1,F0 -- F0 contains a pre-loaded float constant

MULTF F2,F3,F2

ADD R1,R1,16

LD F1,0(R1)

LD F3,-8(R1)

ADDF F6,F3,F1

MULTF F5,F2,F6

ST F5,-16(R1)

BLI R1, 000100000000hex,loop -- compare immediate, branch on less

assuming this code fragment is executed in a statically scheduled pipeline with stages

IF|ID|INT1|INT2| |ME1|ME2|WB

|A1 |A2 |A3|

|M1 |M2 |M3|M4|

|Div1-Div8|

(the Div unit is blocking) and proper forwarding units, assuming that branch instructions take a decision in stage ME2, assuming that all LD hit in L1 D-cache during ME1 (but still go through ME2), and that all ST hit during ME2

b1) show a POE (compiler schedule) that minimizes the clock cycles required to complete execution;

b2) show a ROE for the first iteration of the optimized POE and determine the CPI of the execution of this optimized kernel.

C) The processor runs at 2.6GHz, and has a 64-bit external bus, driven by a memory interface module capable of sustaining 2.2 GT/sec. The external RAM is realized with DDR4 chips (see attached table) and is logically organized with 2 banks, each capable of delivering a 16-bit word. Addressing the memory subsystems requires two bus cycles, and activating a memory row requires 2 bus clock cycles.

c1) Choose a DDR4 module that allows to sustain a burst transfer mode from DDRAM compatible with the memory interface of the processor and estimate the cost of a miss for the above described cache hierarchy;  
c2) discuss possible improvements to the memory subsystem organization to reduce the cost of the miss.

D) Each core of the processor described in A) is organized as a superscalar, 2-way pipeline, that fetches, decodes issues and retires (commits) bundles containing each 2 instructions. The front-end in-order section (fetch and decode) consists of 2 stages. The issue logic takes 1 clock cycle, if the instructions in the bundle are independent, otherwise it takes 2 clock cycles. The architecture supports dynamic speculative execution, and control dependencies from branches are solved when the branch evaluates the condition, even if it is not at commit. The execution model obeys the attached state transition diagram. There is a functional unit (FUs) Int1 for integer arithmetics (arithmetic and local instructions, branches and jumps, no multiplication), 1 FUs FAdd1 for floating point addition/subtraction, 1 FU FMolt1 for floating point multiplication, and a FU for division, FDiv1.

There are 12 integer (R0-R11) and 12 floating point (F0-F11) registers. Speculation is handled through a 8-entry ROB, a pool of 4 Reservation Stations (RS) Rs1-4 shared among all FUs, 2 load buffers Load1 Load2, 1 store buffer Store1 (see the attached execution model): an instruction bundle is first placed in the ROB (if two entries are available), then up to 2 instructions are dispatched to the shared RS (if available) when they are ready for execution and then executed in the proper FU. FUs are *pipelined* (except for the float division unit, which is blocking) and have the latencies quoted in the following table:

|  |  |
| --- | --- |
| Int - 2 | Fadd – 3 |
| Fmolt – 4 | Fdiv – 8 |

Further assumption

* The code is assumed to be already in the I-cache; data caches are described in point A) and are assumed empty and invalidated; the cost of a miss is 40.

d1) assuming a write-back protocol for cache management, show state transitions for all instructions in the first iteration and instructions up to PC04 included in the second iteration :

PC01 ADDI R1,R0,0000FFFFA000hex

PC02 LD F1,0(R1)

PC03 LD F3,8(R1)

PC04 MULTF F2,F1,F0

PC05 MULTF F2,F3,F2

PC06 ADD R1,R1,16

PC07 LD F1,0(R1)

PC08 LD F3,-8(R1)

PC09 ADDF F6,F3,F1

PC10 MULTF F5,F2,F6

PC11 ST F5,-16(R1)

PC12 BLI R1,000100000000hex,PC02

d2) show ROB, RS and buffer status at the issue of PC03 in the second iteration.

Dynamic speculative execution

Decoupled ROB RS execution model

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| **ISTRUCTION** |  |  | **INSTRUCTION STATE** | | | | | | |
|  | **n. ite** | **ROB pos** | **WO** | **RE** | **DI** | **EX** | **WB** | **RR** | **CO** |
| PC01 ADDI R1,R0,0000FFFFA000hex |  |  |  |  |  |  |  |  |  |
| PC02 LD F1,0(R1) |  |  |  |  |  |  |  |  |  |
| PC03 LD F3,8(R1) |  |  |  |  |  |  |  |  |  |
| PC04 MULTF F2,F1,F0 |  |  |  |  |  |  |  |  |  |
| PC05 MULTF F2,F3,F2 |  |  |  |  |  |  |  |  |  |
| PC06 ADD R1,R1,16 |  |  |  |  |  |  |  |  |  |
| PC07 LD F1,0(R1) |  |  |  |  |  |  |  |  |  |
| PC08 LD F3,-8(R1) |  |  |  |  |  |  |  |  |  |
| PC09 ADDF F6,F3,F1 |  |  |  |  |  |  |  |  |  |
| PC10 MULTF F5,F2,F6 |  |  |  |  |  |  |  |  |  |
| PC11 ST F5,-16(R1) |  |  |  |  |  |  |  |  |  |
| PC12 BLI R1, 000100000000hex, PC02 |  |  |  |  |  |  |  |  |  |
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|  | Reservation station and load/store buffers | | | | | | | |
| Busy | Op | Vj | Vk | ROBj | ROBk | ROB pos | Address |
| Rs1 |  |  |  |  |  |  |  |  |
| Rs2 |  |  |  |  |  |  |  |  |
| Rs3 |  |  |  |  |  |  |  |  |
| Rs4 |  |  |  |  |  |  |  |  |
| Load1 |  |  |  |  |  |  |  |  |
| Load2 |  |  |  |  |  |  |  |  |
| Store1 |  |  |  |  |  |  |  |  |
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ROBj ROBk: sources not yet available

ROB pos: ROB entry number where instruction is located

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|  | Result Register status | | | | | | | | | | | | | |
| Integer | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 |  |  |
| ROB pos |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Float. | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 |  |  |
| ROB pos |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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| Reorder Buffer (ROB) | | | | | |
| ROB Entry# | Busy | Op | Status | Destination | Value |
| 0 |  |  |  |  |  |
| 1 |  |  |  |  |  |
| 2 |  |  |  |  |  |
| 3 |  |  |  |  |  |
| 4 |  |  |  |  |  |
| 5 |  |  |  |  |  |
| 6 |  |  |  |  |  |
| 7 |  |  |  |  |  |

CLOCK cycle \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

DI

EX

WB

RR

RE

CO

wo

QUEUE

**Decoupled execution model for bundled (paired) instructions**

The state diagram depicts the model for a dynamically scheduled, speculative execution microarchitecture equipped with a Reorder Buffer (ROB) and a set of Reservation Stations (RS). The ROB and RSs are allocated during the ISSUE phase, denoted as RAT (Register Alias Allocation Table) in INTEL microarchitectures, as follows: a bundle (2 instructions) if fetched from the QUEUE of decoded instructions and ISSUED if there is a couple of consecutive entries in the ROB ( head and tail of the ROB queue do not match); a maximum of two instructions are moved into the RS (if available) when all of their operands are available. Access memory instructions are allocated in the ROB and then moved to a load/store buffer (if available) when operands (address and data, if proper) are available .

**States** are labelled as follows:

WO: Waiting for Operands (at least one of the operands is not available)

RE: Ready for Execution (all operands are available)

DI: Dispatched (posted to a free RS or load/store buffer)

EX: Execution (moved to a load/store buffer or to a matching and free UF)

WB: Write Back (result is ready and is returned to the Rob by using in exclusive mode the Common Data Bus CDB)

RR: Ready to Retire (result available or STORE has completed)

CO: Commit (result is copied to the final ISA register)

**State transitions** happen at the following events:

*from* QUEUE *to* WO: ROB entry available, operand missing

*from* QUEUE *to* RE: ROB entry available, all operands available

*loop at* WO: waiting for operand(s)

*from* WO *to* RE: all operands available

*loop at* RE: waiting for a free RS or load/store buffer

*from* RE *to* DI: RS or load/store buffer available

*loop on* DI: waiting for a free UF

*from* DI *to* EX: UF available

*loop at* EX: multi-cycle execution in a UF, or waiting for CDB

*from* EX *to* WB: result written to the ROB with exclusive use of CDB

*from* EX *to* RR: STORE completed, branch evaluted

*loop at* RR: instruction completed, not at the head of the ROB, or bundled with a not RR instruction

*from* RR *to* CO: bundle of RR instructions at the head of the ROB, no exception raised

**Resources***Register-to-Register* instructions hold resources as follows:

ROB: from state WO (or RE) up to CO, inclusive;

RS: state DI

UF: EX and WB

*Load/Store* instructions hold resources as follows:

ROB: from state WO (or RE) up to CO, inclusive;

Load buffer: from state WO (or RE) up to WB

Store buffer: from state WO (or RE) up to EX (do not use WB)

**Forwarding**: a write on the CDB (WB) makes the operand available to the consumer in the same clock cycle. If the consumer is doing a state transition from QUEUE to WO or RE, that operand is made available; if the consumer is in WO, it goes to RE in the same clock cycle of WB for the producer.

**Branches**: they compute Next-PC and the branch condition in EX and optionally forward Next-PC to the “in-order” section of the pipeline (Fetch states) in the next clock cycle. They do not enter WB and go to RR instead.

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| **Standard  name** | **Memory clock (MHz)** | **I/O bus clock (MHz)** | **Data rate (**[**MT/s**](https://en.wikipedia.org/wiki/Transfer_(computing))**)** | **Module name** | **Peak trans- fer rate (MB/s)** | **Timings CL-tRCD-tRP** | **CAS latency (ns)** |
| DDR4-1600J\* DDR4-1600K  DDR4-1600L | 200 | 800 | 1600 | PC4-12800 | 12800 | 10-10-10 11-11-11 12-12-12 | 12.5  13.75  15 |
| DDR4-1866L\* DDR4-1866M DDR4-1866N | 233.33 | 933.33 | 1866.67 | PC4-14900 | 14933.33 | 12-12-12 13-13-13 14-14-14 | 12.857 13.929 15 |
| DDR4-2133N\* DDR4-2133P DDR4-2133R | 266.67 | 1066.67 | 2133.33 | PC4-17000 | 17066.67 | 14-14-14 15-15-15 16-16-16 | 13.125 14.063 15 |
| DDR4-2400P\* DDR4-2400R DDR4-2400T DDR4-2400U | 300 | 1200 | 2400 | PC4-19200 | 19200 | 15-15-15 16-16-16 17-17-17 18-18-18 | 12.5  13.32  14.16  15 |
| DDR4-2666T DDR4-2666U DDR4-2666V DDR4-2666W | 333.33 | 1333.33 | 2666.67 | PC4-21333 | 21333.33 | 17-17-17 18-18-18 19-19-19 20-20-20 | 12.75  13.50  14.25  15 |
| DDR4-2933V DDR4-2933W DDR4-2933Y DDR4-2933AA | 366.67 | 1466.67 | 2933.33 | PC4-23466 | 23466.67 | 19-19-19 20-20-20 21-21-21 22-22-22 | 12.96  13.64  14.32  15 |
| DDR4-3200W DDR4-3200AA DDR4-3200AC | 400 | 1600 | 3200 | PC4-25600 | 25600 | 20-20-20 22-22-22 24-24-24 | 12.5  13.75  15 |

DDR4 Modules

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