Advanced Computer Architecture  
16-02-2016

A) Let us consider the following code fragment of compiler-unscheduled instructions:

ADDI R1,R0,0000FFFFA000hex -- R1 set to base address 0000FFFFA000hex

loop: LD F1,0(R1)

ADDF F2,F1,F0

MULTF F2,F2,F0

ST F2,0(R1)

ADD R1,R1,16

BLI R1,000100000000hex,loop -- compare immediate, branch on less

assuming this code fragment is executed in a statically scheduled pipeline with stages

IF|ID|INT |MEM|WB

|A1 |A2|A3

|M1 |M2|M3|M4|M5

and proper forwarding units, assuming that branch instructions take a decision in stage MEM, assuming that all LD hit in L1 D-cache with a latency of 2 clock cycles, and that ST hits with a latency of 3 clock cycles

a1) show a compiler schedule that minimizes the clock cycles required to complete execution;

a2) compute the CPI of the execution of this kernel.

B) A server with 128GB RAM is built using 16 processors that embed each four cores that have private L1 caches, while two L2 caches are shared by each couple of cores; the single L3 cache is shared by the four cores. The caches obey the MESI protocol and have the following structure: 32KB, 4-way L1 I-cache and D-cache, each 32-byte block; 1024KB, 4-way associative, 32-byte block L2 cache; 4MB, 8-way associative, 64-byte block shared L3 cache. The latencies (disregarding virtual memory TLB) expressed in clock cycles are: 4 in L1, 8 in L2, 24 in L3. Addresses are 48-bit long. A Ram controller manages the access to a shared bus from each processor. The MESI protocol is enforced throughout the memory hierarchy. A write-back, allocate policy is enforced on the caches.

b1) Core 1) executes the loop of point A above; Core 2) executes the same loop, with the following absolute value for the initial LOAD address 0000FFFFA008hex . Assuming each core starts executing the loop in the same clock cycle, describe the cache events for the execution of the first iteration of each loop, including the MESI states of the involved blocks.

b2) determine the number of hit and miss events for the complete execution of both kernels;

b3) assuming caches are realized with chips hosting 4x1Gbit arrays, determine the number of such chips necessary to set up the caches.

C) The server RAM is built using 2x8GB DDR3 1600 chips attached to the 64-bit external bus of the processors running at 2.6GHz. The external bus allows a maximum transfer rate of 12 GB/sec.

The DDR chips allow reading out a memory word in a single activation, if the memory word is 8 or 16 byte wide; assuming that addressing takes 2 clock cycles and that memory activation takes 2 clocks if the interleaving factor is 2, 4 clocks for an interleaving of 3, and 8 for an interleaving of 4, choose the memory organization (word width and interleaving factor) that minimizes a cache miss, and compute the cost of the miss in processor clock cycles.

D) Each core of the processor is organized as a superscalar, 3-way pipeline, that fetches, decodes issues and retires (commits) bundles containing each 3 instructions. The front-end in-order section (fetch and decode) consists of 2 stages. The issue logic takes 1 clock cycle, if the instructions in the bundle are independent, otherwise it takes 2 clock cycles. The architecture supports dynamic speculative execution, and control dependencies from branches are solved when the branch evaluates the condition, even if it is not at commit. The execution model obeys the attached state transition diagram. There is a functional units (FUs) Int1 for integer arithmetics (arithmetic and local instructions, branches and jumps, no multiplication, 2 FUs FAdd1-Fadd2 for floating point addition/subtraction, two FUs FMolt1-Fmult2 for floating point multiplication, and a FU for division, FDiv1.

There are 12 integer (R0-R11) and 12 floating point (F0-F11) registers. Speculation is handled through a 8-entry ROB, a pool of 4 Reservation Stations (RS) Rs1-4 shared among all FUs, 1 load buffers Load1, 1 store buffer Store1 (see the attached execution model): an instruction bundle is first placed in the ROB (if three entries are available), then up to 2 instructions are dispatched to the shared RS (if available) when they are ready for execution and then executed in the proper FU. FUs are *pipelined* and have the latencies quoted in the following table:

|  |  |
| --- | --- |
| Int - 2 | Fadd – 3 |
| Fmolt – 5 | Fdiv – 6 |

Further assumption

* The code is assumed to be already in the I-cache; data caches are described in point A) and are assumed empty and invalidated; the cost of a miss is 60.

d1) assuming a write-back protocol for cache management, show state transitions for the instructions of the first two iterations of the loop in point A) :

PC01 ADDI R1,R0,0000FFFFA000hex -- R1 set to base address 0000FFFFA000hex

PC02 LD F1,0(R1)

PC03 ADDF F2,F1,F0

PC04 MULTF F2,F2,F0

PC05 ST F2,0(R1)

PC06 ADD R1,R1,16

PC07 BLI R1,000100000000hex,PC02 -- compare immediate, branch on less

d1) show ROB, RS and buffer status at the issue of PC04 in the second iteration;

d2) determine the speed-up that can be obtained by clocking the processor at 3.0 Ghz.

Dynamic speculative execution

Decoupled ROB RS execution model

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **ISTRUCTION** |  |  | **INSTRUCTION STATE** | | | | | | |
|  | **n. ite** | **ROB pos** | **WO** | **RE** | **DI** | **EX** | **WB** | **RR** | **CO** |
| PC01 ADDI R1,R0,0000FFFFA000hex |  |  |  |  |  |  |  |  |  |
| PC02 LD F1,0(R1) |  |  |  |  |  |  |  |  |  |
| PC03 ADDF F2,F1,F0 |  |  |  |  |  |  |  |  |  |
| PC04 MULTF F2,F2,F0 |  |  |  |  |  |  |  |  |  |
| PC05 ST F2,0(R1) |  |  |  |  |  |  |  |  |  |
| PC06 ADD R1,R1,16 |  |  |  |  |  |  |  |  |  |
| PC07 BLI R1,000100000000hex,PC02 |  |  |  |  |  |  |  |  |  |
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|  | Reservation station and load/store buffers | | | | | | | |
| Busy | Op | Vj | Vk | ROBj | ROBk | ROB pos | Address |
| Rs1 |  |  |  |  |  |  |  |  |
| Rs2 |  |  |  |  |  |  |  |  |
| Rs3 |  |  |  |  |  |  |  |  |
| Rs4 |  |  |  |  |  |  |  |  |
| Load1 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| Store1 |  |  |  |  |  |  |  |  |
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ROBj ROBk: sources not yet available

ROB pos: ROB entry number where instruction is located

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | Result Register status | | | | | | | | | | | | | |
| Integer | R0 | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 |  |  |
| ROB pos |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Float. | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 |  |  |
| ROB pos |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| state |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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| Reorder Buffer (ROB) | | | | | |
| ROB Entry# | Busy | Op | Status | Destination | Value |
| 0 |  |  |  |  |  |
| 1 |  |  |  |  |  |
| 2 |  |  |  |  |  |
| 3 |  |  |  |  |  |
| 4 |  |  |  |  |  |
| 5 |  |  |  |  |  |
| 6 |  |  |  |  |  |
| 7 |  |  |  |  |  |

DI

EX

WB

RR

RE

CO

wo

QUEUE

**Decoupled execution model for bundled (paired) instructions**

The state diagram depicts the model for a dynamically scheduled, speculative execution microarchitecture equipped with a Reorder Buffer (ROB) and a set of Reservation Stations (RS). The ROB and RSs are allocated during the ISSUE phase, denoted as RAT (Register Alias Allocation Table) in INTEL microarchitectures, as follows: a bundle (3 instructions) if fetched from the QUEUE of decoded instructions and ISSUED if there is a free triple of consecutive entries in the ROB ( head and tail of the ROB queue do not match); a maximum of two instructions are moved into the RS (if available) when all of their operands are available. Access memory instructions are allocated in the ROB and then moved to a load/store buffer (if available) when operands (address and data, if proper) are available .

**States** are labelled as follows:

WO: Waiting for Operands (at least one of the operands is not available)

RE: Ready for Execution (all operands are available)

DI: Dispatched (posted to a free RS or load/store buffer)

EX: Execution (moved to a load/store buffer or to a matching and free UF)

WB: Write Back (result is ready and is returned to the Rob by using in exclusive mode the Common Data Bus CDB)

RR: Ready to Retire (result available or STORE has completed)

CO: Commit (result is copied to the final ISA register)

**State transitions** happen at the following events:

*from* QUEUE *to* WO: ROB entry available, operand missing

*from* QUEUE *to* RE: ROB entry available, all operands available

*loop at* WO: waiting for operand(s)

*from* WO *to* RE: all operands available

*loop at* RE: waiting for a free RS or load/store buffer

*from* RE *to* DI: RS or load/store buffer available

*loop on* DI: waiting for a free UF

*from* DI *to* EX: UF available

*loop at* EX: multi-cycle execution in a UF, or waiting for CDB

*from* EX *to* WB: result written to the ROB with exclusive use of CDB

*from* EX *to* RR: STORE completed, branch evaluted

*loop at* RR: instruction completed, not at the head of the ROB, or bundled with a not RR instruction

*from* RR *to* CO: bundle of RR instructions at the head of the ROB, no exception raised

**Resources***Register-to-Register* instructions hold resources as follows:

ROB: from state WO (or RE) up to CO, inclusive;

RS: state DI

UF: EX and WB

*Load/Store* instructions hold resources as follows:

ROB: from state WO (or RE) up to CO, inclusive;

Load buffer: from state WO (or RE) up to WB

Store buffer: from state WO (or RE) up to EX (do not use WB)

**Forwarding**: a write on the CDB (WB) makes the operand available to the consumer in the same clock cycle. If the consumer is doing a state transition from QUEUE to WO or RE, that operand is made available; if the consumer is in WO, it goes to RE in the same clock cycle of WB for the producer.

**Branches**: they compute Next-PC and the branch condition in EX and optionally forward Next-PC to the “in-order” section of the pipeline (Fetch states) in the next clock cycle. They do not enter WB and go to RR instead.

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| **Standard name** | **Memory clock**  **(MHz)** | **Cycle time**  **(ns)** | **I/O bus clock**  **(MHz)** | **Data rate**  **(**[**MT/s**](http://en.wikipedia.org/wiki/Transfer_(computing))**)** | **Module name** | **Peak transfer rate**  **(MB/s)** |
| DDR3-800D DDR3-800E | 100 | 10 | 400 | 800 | PC3-6400 | 6400 |
| DDR3-1066E DDR3-1066F DDR3-1066G | 133⅓ | 7 1⁄2 | 533⅓ | 1066⅔ | PC3-8500 | 8533⅓ |
| DDR3-1333F\* DDR3-1333G DDR3-1333H DDR3-1333J\* | 166⅔ | 6 | 666⅔ | 1333⅓ | PC3-10600 | 10666⅔ |
| DDR3-1600G\* DDR3-1600H DDR3-1600J DDR3-1600K | 200 | 5 | 800 | 1600 | PC3-12800 | 12800 |
| DDR3-1866J\* DDR3-1866K DDR3-1866L DDR3-1866M\* | 233⅓ | 4 2⁄7 | 933⅓ | 1866⅔ | PC3-14900 | 14933⅓ |
| DDR3-2133K\* DDR3-2133L DDR3-2133M DDR3-2133N\* | 266⅔ | 3 3⁄4 | 1066⅔ | 2133⅓ | PC3-17000 | 17066⅔ |

DDR3 standard JEDEC specification (source Wikipedia)