Q1) LD R1, (0x 0000 AFAF)

This is a 32-bit (4-byte) load and it should be 4-byte aligned, but it is not. The proper aligned address should be 0000 AFAC (least two significant bits ~~always~~ set to 0).
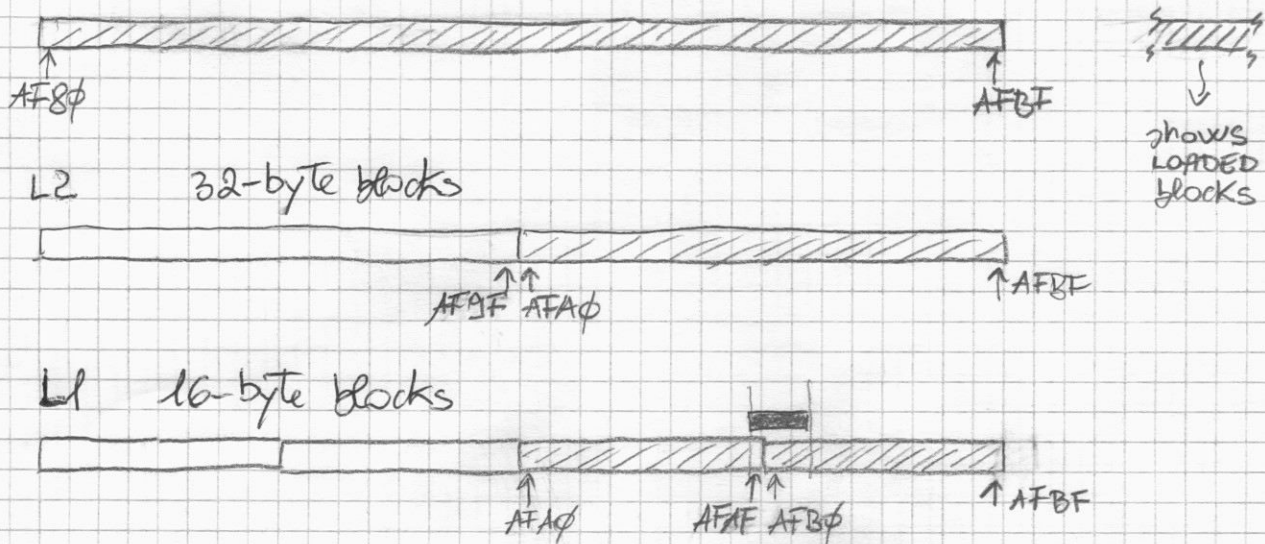
The caches are loaded _always_ from properly aligned memory addresses (L3 64-byte aligned, L2 32-byte and L1 16-byte).

By decomposing 0x 0000 AFAF into its TAG-INDEX-DISP

one obtains the following pattern of blocks for the LD

L3 : 64-byte block   0000 AF80 ÷ 0000 AFBF

shows LOADED blocks

L2   32-byte blocks

L1   16-byte blocks

the LD requires two blocks from L1   4bytes
L1 index : FA first block   FB second block
L2 index : 57D
L3 index : 2BE
Blocks are placed in one of the available ways