a) follows

ST (X), R2   X must be chosen according to
the block placement in L1, L2, L3 as resulting from the
LD R1, (0x0000 AFAF) just described.
Therefore, assuming X is 4-byte aligned

hit L1   0x0000 AFA0 ÷ 0x0000 AFBC
miss L1, hit L2   not possible
miss L1, L2 hit L3   0x0000 AF80 ÷ 0x0000 AF9C
miss L3   X ≤ 0x0000 AF7C ; X ≥ AFC0

B) DDR2 - 1066   bus clock 533 MHz
processor clock 2,33 GHz $\frac{block}{bus\ clock} = \frac{2.33\ 10^9}{533\ 10^6} = 4,37$

L3 cache block = 64 bytes
Memory banks = 2   each 16 bytes $n_{chichous} = \frac{64}{16 \cdot 2} = 2$

$T_{tranf} = 0.5$ (double date rate)

Bus width = 8 bytes

$T_{miss\ (bus\ clock\ cycles)} = T_{add} + n_{activate}\ T_{activat.} + n_{trans}\ T_{transf}$

$= 1 + 2 \cdot 3 + \frac{64}{8} \cdot 0,5 = 1 + 6 + 4 = 11$

$T_{miss\ (processor\ clock\ cycle)} = \lceil 11 \cdot 4,37 \rceil = 49$