Dynamically scheduled, speculative execution – Tomasulo’s algorithm
data structures

De-coupled ROB RS model

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|  | **INSTRUCTION** | **Entry#** | **STATE** |
|  |  | **ROB** | **WO** | **RE** | **DI** | **EX** | **WB** | **RR** | **CO** |
| PC01 | LD F6, 34 (R2) | **1** |  | **1** | **-** | **2-5** | **6** | **7** | **8** |
| PC02 | LD F2, 45 (R3) | **2** |  | **2** |  | **3-6** | **7** | **8** | **9** |
| PC03 | MUL F0, F2, F4 | **3** | **3-6** | **7** | **8** | **9-11** | **12** | **13** | **14** |
| PC04 | SUB F8, F6, F2 | **4** | **4-6** | **7-8** | **9** | **10-12** | **13** | **14** | **15** |
| PC05 | DIV F6, F0, F6 | **1** | **9-11** | **12** | **13** | **14-23** | **24** | **25** | **26** |
| PC06 | ADD F6, F8, F2 | **2** | **10-12** | **13** | **14** | **15-16** | **17** | **18-26** | **27** |
| PC07 | MUL F8, F6, F2 | **3** | **15-16** | **17** | **18** | **19-21** | **22** | **23-27** | **28** |
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**Assumptions:**

1. LD hit in the cache with 4-clock latency;
2. Float ADD and SUB take 2 clock cycles in the EX phase;
3. Float MUL take 3 clock cycles in the EX phase;
4. Fload DIV take 10 clock cycles in the EX phase;
5. RAW dependencies: the producer places its value on the CDB and in the same clock cycle any dependent consumer makes a transition into the RE state;

**Dependencies:**

RAW:

Producer PC01; consumers: PC04,PC05 (F6)

 PC02 PC003,PC04,PC06,PC07 (F2)

 PC03 PC05 (F0)

 PC04 PC06 (F8)

 PC05 none

 PC06 PC07 (F6)

WAR: PC05 (W) after PC04 (R) (F6)

 PC06 (W) after PC05 (R) (F6)

 PC07 (W) after PC06 (R) (F8)

WAW: PC05 (W) after PC01 (W) (F6)

 PC06 (W) after PC05 (W) (F6)

 PC07 (W) after PC04 (W) (F8)

Structural conflicts:

 ROB full

 Single issue to Reservation stations (DI)

 Access to the Common Data Bus (WB)

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|  | Reservation Stations (RS) **at clock 10** |
| Busy | Op | Vj | Vk | ROBj | ROBk | Rob entry | Address |
| Int1 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| FAdd1 | yes | SUB F8,F6,F2 | [load1] | [load2] |  |  | 4 |  |
| FAdd2 | yes | ADD F6,F8,F2 |  | [F2] | 4 |  | 2 |  |
| FMolt1 | yes | MUL F0,F2,F4 | [load2] | [F4] |  |  | 3 |  |
| FMolt2 |  |  |  |  |  |  |  |  |
| FDiv1 | yes | DIV F6,F0,F6 |  | [F6] | 3 |  | 1 |  |
| Load1 |  |  |  |  |  |  |  |  |
| Load2 |  |  |  |  |  |  |  |  |
| Store1 |  |  |  |  |  |  |  |  |
| Store2 |  |  |  |  |  |  |  |  |

ROBj ROBk: sources of operands not yet available

ROB entry: position in the ROB of the instruction

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|  | Result Register status **at clock 10** |
| Int | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 | R13 | R14 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Int | R15 | R16 | R17 | R18 | R19 | R20 | R21 | R22 | R23 | R24 | R25 | R26 | R27 | R28 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Float | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 |
| ROB # | 3 |  |  |  |  |  | 2 |  | 4 |  |  |  |  |  |
| status | B |  |  |  |  |  | B |  | B |  |  |  |  |  |
| Float | F14 | F15 | F16 | F17 | F18 | F19 | F20 | F21 | F22 | F23 | F24 | F25 | F26 | F27 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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| Reorder Buffer (ROB) **at clock 10** |
| Entry # | Busy | Op | State | Destination | Value |
| 1 | yes | DIV F6,F0,F6 | WO | *F6 cancelled* |  |
| 2 | yes | ADD F6,F8,F2 | WO | F6 |  |
| 3 | yes | MUL F0,F2,F4 | EX | F0 |  |
| 4 | yes | SUB F8,F6,F2 | EX | F8 |  |
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head: next instruction to be retired/committed

tail: first slot for incoming new instruction

If head and tail coincide (3), ROB is full, structural conflict

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|  | Reservation Stations (RS) **at clock 15** |
| Busy | Op | Vj | Vk | ROBj | ROBk | Rob entry | Address |
| Int1 |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |
| FAdd1 |  |  |  |  |  |  |  |  |
| FAdd2 |  |  |  |  |  |  |  |  |
| FMolt1 |  |  |  |  |  |  |  |  |
| FMolt2 |  |  |  |  |  |  |  |  |
| FDiv1 |  |  |  |  |  |  |  |  |
| Load1 |  |  |  |  |  |  |  |  |
| Load2 |  |  |  |  |  |  |  |  |
| Store1 |  |  |  |  |  |  |  |  |
| Store2 |  |  |  |  |  |  |  |  |

ROBj ROBk: sources of operands not yet available

ROB entry: position in the ROB of the instruction

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| --- | --- |
|  | Result Register status **at clock 15** |
| Int | R1 | R2 | R3 | R4 | R5 | R6 | R7 | R8 | R9 | R10 | R11 | R12 | R13 | R14 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Int | R15 | R16 | R17 | R18 | R19 | R20 | R21 | R22 | R23 | R24 | R25 | R26 | R27 | R28 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Float | F0 | F1 | F2 | F3 | F4 | F5 | F6 | F7 | F8 | F9 | F10 | F11 | F12 | F13 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Float | F14 | F15 | F16 | F17 | F18 | F19 | F20 | F21 | F22 | F23 | F24 | F25 | F26 | F27 |
| ROB # |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| status |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

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| Reorder Buffer (ROB) **at clock 15** |
| Entry # | Busy | Op | State | Destination | Value |
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If head and tail coincide (3), ROB is full, structural conflict